ATTACHMENT A OF REISSUE APPLICATION DECLARATION
BY ASSIGNEE (FORM PTO/SB52)

... Claim 1 is arguably subject to an incorrect interpretation that the "packaged integrated circuit" could be mounted on a substrate or the like with the "back surface" of the die facing towards the substrate so that the "protective film" would be disposed intermediate the "die" and the substrate.

Prior art exists disclosing a die mounted on the substrate by way of some adhering agent, such as an adhesive, where the adhering agent could possibly be considered to be the claimed "protective film". See, for example, USPNo. 5,504,374 that issued on April 2, 1996 and entitled "Microcircuit Package Assembly Utilizing Large Size Die and Low Temperature Curing Organic Die Attach Material". This prior art patent discloses a die 14 mounted on a substrate 12 by way of an adhesive die attach 16. Thus, such prior art places the validity of Claim 1 in some doubt when the claim is interpreted in the manner described above.

Claim 1 is being amended by way of the enclosed Amendment referenced above to recite that the "first surface of the die" includes a "plurality of electrical contact bumps" such as bumps 106 depicted in Fig. 2 of the subject reissue application. Prior art packaged integrated circuits having "contact bumps" are mounted with the bumps adjacent a supporting substrate on a substrate or the like with the "contact bumps" facing the substrate so that the claimed "protective film" would not be disposed between the "die" and the substrate. Prior art flip-chip circuits utilize contact bumps such as disclosed in USPNo. 5,311,059 issued on May 10, 1994 and entitled "Backplane Grounding for Flip-Chip Integrated Circuit". This patent discloses the use of a metallic coating 14 on what could be considered to be the "back surface" of the chip 10 which functions as a ground

plane for the chip. However, Claim 1 recites that the thickness of the "protective layer" is between 1.5 and 5 mils, and there is no teaching regarding the thickness of the metallic coating 14 of this prior art patent.

New Claims 7 – 10 have been added by way of the Amendment referenced above. These claims all depend from Claim 1 and thus further limit the claim.

New Claim 11 has been added which is also directed to a packaged integrated circuit. A "protective film" is included which again is disposed on a "back surface" of a "die". The "protective film" includes "laser identification markings". The prior art noted above does not disclose an adhering agent or the like which could be construed as a "protective film" and which further includes "laser identification markings" as recited in new Claim 11. New Claims 12 – 15 depend, either directly or indirectly, from independent Claim 11 and thus further limit the claim.

ATTACHMENT B OF REISSUE APPLICATION DECLARATION
BY ASSIGNEE (FORM PTO/SB52)

Power Of Attorney, continued:

Name(s):	Registration Number:
Coleman F. Reif	38,593
Allen R. Tremain	40,207
Andrew S. Viger	28,552
Peter Y. Wang	40,452
Philip A. Girard	28,848
Alfred A. Equitz	30,922

ATTACHMENT C OF REISSUE APPLICATION DECLARATION
BY ASSIGNEE (FORM PTO/SB52)

Patentees, continued:

Patentee: Nikhil Vishwanath Kelkar Citizenship: India
Residence/Mailing Address: 6385 Lillian Way, San Jose, CA 95120

Express Mail Number EL 727719571 US

PTO/SB/52 (02-01)
Approved for use through 01/31/2004. OMB 0651-0033
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REISSUE APPLICATION DECLARATION BY THE ASSIGNEE

Docket Number (optional): NSC1-G9900

I hereby declare that:

My residence and mailing address and citizenship are stated below next to my name.

I am authorized to act on behalf of the following assignee: National Semiconductor Corporation

and the title of my position with said assignee is: Member of the Technical Staff of the Intellectual Property Group

The entire title to the patent identified below is vested in said assignee.

Name of Patentee(s): Pai-Hsiang Kao, et al.

Patent Number	Date of Patent Issued
6,023,094	February 8, 2000

Title of Invention: Semiconductor Wafer Having A Bottom Surface Protective Coating

I believe said patentee(s) to be the original, first and sole/joint inventor(s) of the subject matter which is described and claimed in said patent, for which a reissue patent is sought on the invention entitled Semiconductor Wafer Having A Bottom Surface Protective Coating,

the specification of which

[X] is attached hereto, together with the accompanying Preliminary Amendment.

[ ] was filed on _____ as reissue application number ____ /_____
and was amended on _____
(If applicable)

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

[ ] by reason of a defective specification or drawing.

[X] by reason of the patentee claiming more or less than he had the right to claim in the patent.

[ ] by reason of other errors.

At least one error upon which reissue is based is described as follows:

Claim 1 of the original patent recites that the claimed "packaged integrated circuit" includes a "protective film adhered directly to a back surface of ... [a] die"... (See Attachment A to Reissue Application Declaration)

[Attach additional sheets, if needed.]

All errors corrected in this reissue application arose without any deceptive intention on the part of the applicant.

PTO/SB/52 (02-01)
Approved for use through 01/31/2004. OMB 0651-0033
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REISSUE APPLICATION DECLARATION BY THE ASSIGNEE

Docket Number (Optional): NSC1-G9900

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith.

Name(s)	Registration Number
Christopher J. Byrne	32,204
Eugene C. Conser	39,149
John Maxim	34,688

(Continued on Attachment B to Reissue Application Declaration)

Correspondence Address: Direct all communications about the application to:

☐ Customer Number [ ] *Type Customer Number Here* → *Place Customer Number Bar Code Label Here*

OR

☒ Firm or Individual Name	Philip A. Girard c/o Girard & Equitz LLP				
Address	400 Montgomery Street, Suite 1110				
Address					
City	San Francisco	State	CA	Zip	94104
Country	United States				
Telephone	(415) 433-2250	Fax	(415) 433-2255		

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

Full name of person signing (given name, family name)
Allen R. Tremain

Signature: Allen R. Tremain | Date: November 30, 2001

Address of Assignee
2900 Semiconductor Drive, Santa Clara, CA 95052

Patentee: Pai-Hsiang Kao	Citizenship: Taiwan
Residence/Mailing Address: 19445 Dorchester Dr., Saratoga, CA 95070	
Patentee: William Jeffrey Schaefer	Citizenship: United States
Residence/Mailing Address: 7589 Silvertree Ln., Dublin, CA 94568	

☒ Additional Patentees are named on separately numbered sheets attached hereto. (See Attachment C to Reissue Application Declaration)

Express Mail Number EL 727719571 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reissue Application of

PAI-HSIANG KAO, et al.

Patent No. 6,023,094

Issued: February 8, 2000

For: **SEMICONDUCTOR WAFER HAVING A BOTTOM SURFACE PROTECTIVE COATING**

CONSENT BY ASSIGNEE TO FILING OF REISSUE APPLICATION AND OFFER TO SURRENDER ORIGINAL PATENT

400 Montgomery Street, Suite 1110
San Francisco, CA 94104
(415) 433-2250

Box Reissue
Commissioner for Patents
Washington, D.C. 20231

Sir:

National Semiconductor Corporation, assignee of U.S. Patent No. 6,023,094 by assignment records at reel 8951, frame 0774 on January 14, 1998, consents to the filing of the present application for the reissue of U.S. Patent No. 6,023,094.

Further, National Semiconductor Corporation hereby offers to surrender U.S. Patent No. 6,023,094 pursuant to 37 CFR § 1.178(a).

The undersigned (whose title is supplied below) is authorized to act on behalf of National Semiconductor Corporation in this matter.

Dated: 10/11/01

By: _____

Name: Christopher J. Byrne

Title: Director of Intellectual Property and Technology Licensing

Attorney Docket No. NSC1-G9900